34. (New) A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

35. (New) A semiconductor device as recited in claim 34, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

REMARKS

The Examiner is thanked for the careful review of this Application. In response to the Office Communication, restriction requirement dated February 4, 2003, Applicants hereby elect, without traverse, claims 6-8 and 26-35, directed to the species directed to the embodiments of Figures 1F-2 and 1F-3, to prosecute in the above-identified Patent Application. The claim amendments provided herein assume entry of all prior amendments. Claims 6-8 and 26-35 are pending after entry of the present Amendment. Please add new claims 26-35 and cancel claims 1-6 and 22-25. New claim 26 corresponds to claim 21 added via Amendment filed on July 24, 2002. Claim 21 was previously cancelled in the Response to Restriction Requirement filed on November 22, 2002. These amendments therefore place the case in condition for proper examination in view of the elected species. These amendments do not introduce any new matter.

In view of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Gotkis et al.

Application No: 09/821,415

Filed: March 28, 2001

For: SEMICONDUCTOR STRUCTURE IMPLEMENTING LOW-K DIELECTRIC MATERIALS AND SUPPORTING STUBS (As Amended)

Atty. Docket: LAM2P246

Examiner: H.K. Vu

Group Art Unit: 2811

Date: February 28, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on February 28, 2003.

Signed: _____
Kay Harlow

MARKED UP CLAIMS

26. **(New)** A semiconductor device as recited in claim 6, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

27. **(New)** A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs further support the passivation layer.

28. **(New)** A semiconductor device, comprising:

a substrate having transistor devices; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper

interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

29. **(New)** A semiconductor device as recited in claim 28, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

30. **(New)** A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

31. **(New)** A semiconductor device as recited in claim 28, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

32. **(New)** A semiconductor device as recited in claim 28, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

33. **(New)** A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs further support the passivation layer.

34. **(New)** A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

35. **(New)** A semiconductor device as recited in claim 34, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.